Amendments to the Drawings:

The attached sheets of drawings include changes to Figure 2 and new Figures 7-10.

Attachments: 1 Replacement Sheet and 4 New Sheets.

REMARKS

Claims 1, 3-11 and 13-42 and 45-49 are currently pending in this application. Claims 1, 3-11 and 13-42, 45 and 46 have been rejected. The Examiner objected to claims 43 and 44, but indicated claims 43 and 44 were directed to allowable subject matter, and would be allowable if restated in independent form. The Examiner is thanked for indicating that claims 43 and 44 were directed to allowable subject matter. Claims 47-49 are new and are directed to the subject matter of claims 43 and 44 that the Examiner indicated was allowable. Claims 43 and 44 have been canceled.

As an initial matter, Applicants respectfully submit that the office action was improperly made final. The Examiner did not address Applicants' arguments regarding the allowable subject matter of claims 1 and 3-10. Instead, the Examiner issued a rejection of these claims under 35 U.S.C. § 112 as indefinite. As discussed in more detail below (and as is clear from the Examiner's own analysis on page 7 of the Final Office Action), one of skill in the art would not have been confused as to whether the input module or the third control circuit sets the match signal. Thus, unless the Examiner is prepared to allow claims 1 and 3-10 once the informalities are corrected, the Examiner improperly relied on a minor rejection as to form to avoid addressing the merits. *See* MPEP § 707.07(g) ("In cases where there exists a sound rejection on the basis of prior art which discloses the "heart" of the invention ... secondary rejections on minor technical grounds should ordinarily not be made."). *See also* MPEP § 707(e) ("As soon as allowable subject matter is found, correction of all informalities then present should be required"), and (f) ("Whenever the requirements are traversed ... the examiner should make proper reference thereto in his or her action on the merits"); 37 C.F.R. §§ 1.104 and 1.113 ("In making such final rejection, the examiner shall repeat or state all grounds of rejection then considered applicable to the claims in the application, clearly stating the reasons in support thereof."). Accordingly, Applicants respectfully request that the Examiner withdraw the finality of the Office Action.

Objections to the Drawings

The Examiner objected to the drawings under 37 C.F.R. § 1.121(d) for failing to show every feature of the invention specified in the claims. Applicants respectfully traverse the Examiner's objections.

With regard to claims 1, 10 and 11, the Examiner contends the claimed first control circuit is not illustrated in the figures. An embodiment of the first control circuit is illustrated in Figure 2 as the main processor 600. No new matter has been introduced. See Original Specification at page 15-16, in particular, see the paragraph beginning on page 15 and continuing on page 16 of the Original Specification (the paragraph beginning on page 13, line 26 of the Substitute Specification), which discusses the main processor 600.

With regard to claims 11, 13-15, 18-20, 30-33 and 36-37, the Examiner contends the methods are not illustrated in the drawings. New Figures 7-10 illustrate example embodiments of the claimed methods. No new matter has been introduced. See Original Specification: Summary of the Invention at 5-6 (Substitute Specification at 4-5); page 16, line 18 through page 27, line 5 (Substitute Specification at 14, line 11 through 23, line 15).

Claim Rejections Under 35 U.S.C. § 112

The Examiner has rejected Claims 1 and 3-10 under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement. Specifically, the Examiner contends the claims are indefinite because it is unclear whether the third control circuit or the first control circuit sets the match signal. Applicants respectfully traverse the Examiner's rejections. Independent claims 1 and 10 (both before and after amendment), recite "a third control circuit ... for setting a match signal." The Examiner's own analysis on page 7 of the Final Office Action states "the particular match signal as disclosed in the specification and required by the claim to be generated by the 'third control circuit.'" Thus, there is no confusion about whether the input module or the third control circuit sets the match signal. Nevertheless, Applicants have amended claims 1 and 10 to eliminate any possible ambiguity. No change in claim scope is intended. Claims 3-9 depend from claim 1. Thus, Applicants submit that claims 1 and 3-10 are sufficiently definite.

Where the Examiner has not cited any prior art against claims 1 and 3-10, and has not addressed Applicants' prior arguments that claims 1 and 3-10 are not anticipated or rendered obvious by the art previously cited by the Examiner, Applicants respectfully submit that claims 1 and 3-10 are allowable. *See* MPEP § 707(f) (applicant's arguments should be rebutted to avoid implication that they should be accepted at face value), and (g) (piecemeal examination should be avoided).

In any event, claims 1 and 3-10 are not anticipated or rendered obvious by U.S. Patent No. 5,521,979 issued to Deiss for the reasons set forth in Applicants' Supplemental Amendment of May 9, 2005 on pages 13-15. The Examiner does not address these reasons in the Final Office Action. Further, claims 1 and 3-10 are not anticipated or rendered obvious by U.S. Patent No. 5,959,659 issued to Dokic because Dokic, alone or in combination with the ADSP-2100 Family User's Manual – Chapter 4: Data Transfer ("the Manual"), for the reasons set forth in Applicants' Supplemental Amendment of May 9, 2005, on pages 18-19. The Examiner does not address these reasons with respect to claims 1 and 3-10 in the Final Office Action. In addition, the arguments regarding the data buffers of Dokic and the Manual and set forth below with respect to claims 11 and 13-20 similarly apply to claims 1 and 3-10. Accordingly, Applicants respectfully submit that claims 1 and 3-10 are not anticipated or rendered obvious by the cited references.

Claim Rejections Under 35 U.S.C. § 102

The Examiner has rejected Claims 39-41, 45 and 46 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 5,959,659 issued to Dokic. Applicants respectfully traverse the Examiner's rejections.

Independent claim 39 recites: "A receiver ... comprising: an input module to receive and process a data packet; a memory; a receiver processor to control storage of desired packet identifiers and associated control information in the memory; and a transport controller having a transport processor to extract a packet identifier from a packet in the input module and a search engine to search the memory for a match of the extracted packet identifier to a desired packet identifier stored in the memory, wherein responsive to a match the transport processor

retrieves from the memory control information associated with the desired packet identifier stored in the memory and controls processing of the received data packet by the input module based on the retrieved control information. Claims 40 and 41 depend from claim 39.

The Examiner points to demultiplexer section 104 as the claimed input module, memory 205 as the claimed memory, host processor 106 as the claimed receiver processor, and digital signal processor 102 as the claimed transport processor, and to the description thereof at column 7, l. 49, through col. 9, l. 6, and col 13, ln. 13-26.

There is no indication in the cited portion of Dokic that the host processor 106 controls storage of desired packet identifiers ***and*** associated control information in the memory 205. The cited portion of Dokic refers to loading a PID filtering table from the host processor 106 into the memory 205. Dokic then defines the PID filtering table as containing the desired PIDs. There is no suggestion that the PID filtering table contain associated control information, or that such information be stored anywhere else in the memory 205. *See* Dokic, column 8, ln. 26-53. In addition, there is no indication in the cited portion of Dokic that the digital signal processor 102, responsive to a match, retrieves from the memory 205 control information associated with the desired packet identifier. Accordingly, Dokic does not anticipate claims 39-41.

To the extent the Examiner suggests that the type of packet is the "associated control information," Dokic does not teach, suggest or motivate storing the type of packet in the memory 205 (or retrieving the type of packet from the memory 205). Instead, Dokic teaches that the location in the PID filtering table where the PID is stored corresponds to the type of data packet. To the extent the Examiner points to the discussion of selecting a default program in Dokic (see col. 8, ln. 53-67), the default program data in Dokic is recovered from the transport stream when a PID filtering table is not available from the host processor 106. There is no suggestion in Dokic that the host processor 106 controls the storage of default PIDs in the memory 205 (or the storage of associated control information in the memory 205).

Independent claim 45 separately recites: "means for receiving a data packet in the digital data stream; means for retrieving control information associated with a received data packet; and means for controlling processing of a received data packet by the means for

receiving a data packet." As discussed above, Dokic does not teach, motivate or suggest retrieving control information associated with a received data packet. Claim 46 depends from claim 45 and further specifies that the means for retrieving control information comprises "a memory storing packet identifiers and control information associated with desired data packets in the digital data stream, a search engine and a transport processor." Accordingly, Applicants respectfully submit that claims 39-41, 45 and 46 are not anticipated by Dokic.

Claim Rejections Under 35 USC § 103

The Examiner has rejected Claims 11 and 13-20 under 35 USC 103(a) as rendered obvious over Dokic in view of the ADSP-2100 Family User's Manual – Chapter 4: Data Transfer. Applicants respectfully traverse the Examiner's rejection.

Independent claims 11 and 20 recite, "inputting the digital data stream; storing in a memory separate from the data stream and under the control of a first control circuit, packet identifiers of data packets required by the receiver; extracting, under the control of a second control circuit, a packet identifier from a data packet in the input digital data stream; determining, under the control of a third control circuit, whether the extracted packet identifier matches one of the stored packet identifiers; setting a match signal responsive to a match determined by the third control circuit; outputting, responsive to a match and under the control of the third control circuit, an address in the memory; accessing, under the control of the second control circuit, the address in memory; retrieving control information associated with the packet identifier and stored at such address; and demultiplexing, under the control of the second control circuit, the input data packet responsive to the match signal," (or similar language).

As previously noted, Dokic is not an appropriate primary reference because the Examiner is using an unreasonable interpretation of the claimed memory to include the memory 205 **and** data buffers 200 and 202 of Dokic. Buffers 200 and 202 are not separate from the data stream and do not store "packet identifiers corresponding to data packets required by the receiver" for determining "whether the extracted packet identifier matches one of the stored packet identifiers." Buffers 200 and 202 are circular buffers controlled by framing logic to load **all** data packets in the transport stream, whether the packets are required or not. See Column 7,

line 66 to Column 8, line 19. Thus, buffers 200 and 202 are not separate from the data stream. Thus, Dokic is not an appropriate primary reference for claims 11 and 13-20.

The Examiner first argues that the buffers 200 and 202 meet the claim limitations for the memory if they store desired packet identifiers even for an instant. The Examiner ignores the limitation that the memory storing the packet identifiers be "separate from the data stream." The Examiner next argues that the specification discloses buffers in the data stream and storage of data packets from the data stream in the memory. The Examiner fails to provide specific citations to the specification and does not tie this argument to corresponding limitations in the claims. In any event, the specification as originally filed separately illustrates and describes the data stream. *See, e.g.* Original Specification, Figures 1 and 2 and the description thereof on pages 7-12. An embodiment of the data stream is illustrated and described as comprising the transport stream 1, the input module 100, interconnect 108, interconnect 110, the alternative output stream 106, the transport controller 200, the interconnect 502, the direct memory access controller 500 and the data output stream 506. See Figures 2 and 3. The specification as originally filed also separately illustrates and describes the data SRAM 400. *See, e.g.*, Figure 2 and the description of the data SRAM 400 on pages 11-13. There is no suggestion that the data stream or the transport stream includes the data SRAM 400, passes through the data SRAM 400, or is buffered in the data SRAM 400, and Applicants respectfully submit one of skill in the art would not interpret the specification in this manner. Applicants further note that the claims do not address whether the transport stream comprises input buffers, or prohibit the memory from also storing data packets (or portions thereof).

Further, and as previously noted, the Examiner admits that Dokic does not disclose or suggest "outputting an address", but claims this is suggested by the Manual, which describes the operation of a circular buffer. The problem with this argument is that the circular buffer of Dokic that the Examiner suggests combining with the Manual is the circular buffer 200/202, which the Examiner admits stores the "entire packet" and which as discussed above cannot be the claimed memory as recited. Accordingly, Applicants respectfully submit claims 1, 3-11, 13-20 and 39-46 are not rendered obvious by Dokic taken in combination with the Manual. Furthermore, if Dokic were modified such that the circular buffers stored either packet identifiers

required by the receiver or addressing information, Dokic would not function as intended, as the stored information would be replaced (and thus lost) if the buffers were operated in a circular fashion and there would be no place to store the digital data stream as it was received if the buffers were not operated in a circular fashion or were used to store other information. Further, to the extent the address is an address of one of the buffers, it is still an address of a buffer in the data stream, and thus would not be an address in a memory separate from the data stream, as recited. The Examiner fails to address these arguments in the Final Office Action. Accordingly, Applicants respectfully submit that claims 11 and 13-20 are not rendered obvious by the combination of Dokic and the Manual.

The Examiner rejected Claims 21-38 under 35 U.S.C. § 103(a) as rendered obvious by Dokic in view of U.S. Patent No. 5,844,595 issued to Blatter et al. Applicants respectfully traverse the Examiner's rejections.

Claims 21 and 29 recite "a first data structure for storing addressing information that is accessed based on packet identifiers ... a second data structure for storing control information that is accessed based on addressing information extracted from the first data structure ... outputting addressing information responsive to a match ... wherein the first control circuit accesses the second data structure to retrieve control information associated with the addressing information." Similarly, claim 30 recites ""storing control information in a first data structure; storing packet identifiers and corresponding addressing information in a second data structure ... outputting addressing information from the second data structure responsive to a match [and] retrieving ... based on the outputted addressing information, control information from the first data structure" and claim 38 similarly recites "storing, in a first data structure, control information; storing, in a second data structure, packet identifiers ... and addressing information corresponding to the packet identifiers ... outputting, responsive to a match, addressing information stored in the second data structure [and] retrieving ... based on the outputted addressing information, control information from the first data structure."

The Examiner admits that Dokic does not disclose or suggest the claimed first and second data structures. The Examiner contends memory 205 of Dokic is a first data structure, without explaining how or whether it satisfies the claim limitations. The Examiner also points to

units 45 of Blatter as both the first data structure and the second data structure. The Examiner does not identify how to combine unit 45 with Dokic so as to achieve the claimed invention. Further, one of skill in the art would not be motivated to combine Dokic with Blatter. Dokic is directed to "a decoder having a decoupled hardware architecture for demultiplexing and decoding a digital data stream." Dokic, Column 1, lines 6-9. Dokic specifically decouples demultiplexing from decoding the digital data stream and expressly limits the "interpretation capabilities" of the digital signal processor 102 in order to speed up the demultiplexing so data can promptly be displayed. Dokic, Column 4, lines 48-60. The only data Dokic indicates is stored in the memory 205 is the PID look-up table, which Dokic teaches preferable contains only the required PIDs. There is no teaching or suggestion in Dokic that the PID look-up table contain addressing information that is accessed based on packet identifiers or control information that is accessed based on addressing information. Modifying the digital signal processor 102 of Dokic to contain two data structures with the second data structure containing control information to be retrieved and either employed by the digital signal processor to interpret the data stream or provided to an external circuit by the digital signal processor would defeat the purpose of limiting the capabilities of the digital signal processor in order to speed up the demultiplexing, and would change the principles of operation of Dokic. *See* MPEP § 2143.01(VI) ("The proposed modification cannot change the principle of operation of a reference."); *In re Ratti*, 270 F.2d 810, 813, 123 U.S.P.Q. 349, 352 (C.C.P.A. 1959). Claims 22-28 depend from claim 21 and claims 31-37 depend from claim 30. Accordingly, Applicants submit that claims 21-38 are not rendered obvious by Dokic in view of Blatter.

The Examiner rejected Claim 42 under 35 U.S.C. § 103(a) as being unpatentable over Dokic in view of U.S. Patent No. 5,602,920 issued to Bestler et al. Applicants respectfully traverse the Examiner's rejection. Claim 42 depends from claim 39. The Examiner does not contend that the features of claim 39 that are missing from Dokic, as discussed above, are taught, suggested or motivated by Bestler. Accordingly, Applicants respectfully submit that claim 42 is not rendered obvious by the combination of Dokic and Bestler.

New Claims

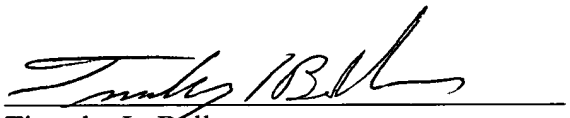
Applicant has added new claim 47 to claim embodiments directed to the subject matter the Examiner indicated was allowable. New claims 48 and 49 depend from claim 47. Accordingly, Applicants respectfully submit that claims 47-49 are allowable.

The Director is authorized to charge any additional fees due by way of this Amendment, or credit any overpayment, to our Deposit Account No. 19-1090.

All of the claims remaining in the application are now clearly allowable. Favorable consideration and a Notice of Allowance are earnestly solicited.

Respectfully submitted,

SEED Intellectual Property Law Group PLLC



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Enclosures:
5 Sheets of Drawings (Replacement Sheet of Figure 2 and New Sheets for Figures 7-10)

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